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Claims

[c1] 1. A method of preparing a substrate for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:
conducting a first non-selective etch on the surface of a silicon carbide substrate to remove both surface and subsurface damage;
thereafter conducting a selective etch on the same surface sufficient to delineate the basal plane dislocations with the wafer surface and that will thereafter tend to terminate or to propagate as threading defects while avoiding creating beta (3C) inclusions and carrot defects;
growing a conductive epitaxial layer on the selectively etched substrate surface to a thickness greater than that of the typical threading dislocation etch pit depth in the selectively-etched surface to thereby provide the epitaxial layer with a sufficient thickness to support additional polishing and etching steps above the substrate;
polishing away a sufficient portion of the conductive epitaxial layer to remove the material containing the etched pits to thereby provide a surface with fewer etched pits than the surface of the selectively-etched substrate; and

conducting a second non-selective etch of the epilayer sufficient to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward voltage in a device formed on the substrate and the polished epilayer.

[c2] 2. A substrate-preparation method according to Claim 1 wherein the step of conducting the first isotropic etch comprises conducting a reactive ion etch.

[c3] 3. A substrate-preparation method according to Claim 1 wherein the step of conducting the selective etch comprises etching the surface with a molten salt.

[c4] 4. A substrate-preparation method according to Claim 3 comprising etching the surface with molten potassium hydroxide.

[c5] 5. A substrate-preparation method according to Claim 1 further comprising forming a bipolar device by:
forming a n-type epitaxial layer above the polished and etched surface of the epitaxial layer; and
forming a p-type epitaxial layer above the polished and etched surface of the epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

[c6] 6. A device-preparation method according to Claim 5 comprising:
etching an n-type silicon carbide substrate;
growing, polishing and etching an n epitaxial layer on the selectively etched substrate surface;
growing another n-type epitaxial layer above the polished and etched epitaxial layer; and
growing a p-type epitaxial layer above the n-type epitaxial layer, with a p-n junction between the n-type and p-type epitaxial layers.

[c7] 7. A method according to Claim 1 and further comprising the steps of sawing a silicon carbide substrate wafer from a silicon carbide boule; and thereafter conducting the nonselective etch on the substrate wafer.

[c8] 8. A method according to Claim 7 and further comprising lapping and polishing the sawed substrate wafer and prior to conducting the nonselective etch.

[c9] 9 A method according to Claim 8 comprising growing the first device epitaxial layer immediately on the surface prepared by the second non-selective etch.

[c10] 10. A method according to Claim 1 comprising conducting the non-selective and selective etches on a single crystal silicon carbide substrate having a polytype se-

lected from the 3C, 4H, 6H and 15R polytypes of silicon carbide.

[c11] 11. A method of preparing a substrate and epilayer for reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:
etching the surface of a silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage;
thereafter etching the same surface with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface; and thereafter
growing a first epitaxial layer of silicon carbide on the twice-etched surface.

[c12] 12. A method according to Claim 11 comprising etching the surface with a reactive ion etch as the nonselective etch.

[c13] 13. A method according to Claim 11 comprising etching the surface with a chemical mechanical polishing step.

[c14] 14. A method according to Claim 11 comprising etching

the surface with a molten salt as the selective etch.

[c15] 15. A method according to Claim 11 comprising growing a conductive epitaxial layer on the twice-etched surface.

[c16] 16. A method according to Claim 15 comprising growing an n-type epitaxial layer on the twice-etched surface.

[c17] 17. A method according to Claim 11 comprising growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer.

[c18] 18. A method according to Claim 11 wherein the step of growing the first epitaxial layer comprises forming a semi-sacrificial epitaxial layer on the selectively etched surface to encourage the etched basal plane defects to reorient during subsequent growth into threaded defects;
and further comprising the steps of:
polishing the etched semi-sacrificial epitaxial layer to reduce etch pits; and
etching the polished semi-sacrificial epitaxial layer to remove subsurface damage from the step of polishing the epitaxial layer but without reaching the underlying substrate, to thereby reduce the number of subsurface defects that can propagate stacking faults under forward

voltage in a device formed on the substrate and the polished epilayer;
all prior to forming the first epitaxial layer.

[c19] 19. A method according to Claim 18 comprising forming the semi-sacrificial layer by chemical vapor deposition.

[c20] 20. A method according to Claim 18 comprising polishing the etched semi-sacrificial epitaxial layer using a chemical-mechanical process.

[c21] 21. A method according to Claim 18 comprising etching the polished semi-sacrificial epitaxial layer using a dry etch.

[c22] 22. A method according to Claim 21 comprising etching the polished semi-sacrificial epitaxial layer using a reactive ion etch.

[c23] 23. A method according to Claim 11 and further comprising the steps of:
sawing the substrate from a single crystal boule;
lapping the sawed substrate;
polishing the lapped substrate; and
cleaning the polished substrate;
all prior to the nonselective etch.

[c24] 24. A method of preparing a substrate and epilayer for

reducing stacking fault nucleation and reducing forward voltage (V_f) drift in silicon carbide-based bipolar devices, the method comprising:

etching the surface of a silicon carbide substrate from which surface and subsurface damage have been removed with a selective etch to thereby develop etch-generated structures from at least any basal plane dislocations on the substrate that will thereafter tend to either terminate or to propagate as threading dislocations during subsequent epilayer growth on the substrate surface; and thereafter

growing a first conductive epitaxial layer of silicon carbide on the twice-etched surface.

[c25] 25. A method according to Claim 24 comprising etching the surface of the silicon carbide substrate with a nonselective etch to remove both surface and subsurface damage prior to the step of etching the surface with the selective etch.

[c26] 26. A method according to Claim 25 and further comprising the steps of:

sawing the substrate from a single crystal boule;

lapping the sawed substrate;

polishing the lapped substrate; and

cleaning the polished substrate;

all prior to the nonselective etch.

[c27] 27. A method according to Claim 25 comprising etching the surface with a reactive ion etch as the nonselective etch.

[c28] 28. A method according to Claim 25 comprising etching the surface with a chemical mechanical polishing step as the nonselective etch.

[c29] 29. A method according to Claim 24 comprising etching the surface with a molten salt as the selective etch.

[c30] 30. A method according to Claim 24 comprising growing a second conductive epilayer above the first conductive epilayer and having the opposite conductivity type from the first conductive epilayer.